#8
J. Douglas
12/17/03

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Applicant:	Paul S. Gryskiewicz	Art Unit:	2614
Serial No.:	09/652,694	Examiner:	Brian P. Yenke
Filed:	August 31, 2000		
For:	Adaptive Video Scaler	Atty Docket:	ITL.0447US P9445

Mail Stop **Appeal Brief-Patents**
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPEAL BRIEF

Sir:

Applicant respectfully appeals from the final rejection mailed June 6, 2003.

I. REAL PARTY IN INTEREST

The real party in interest is the assignee Intel Corporation.

II. RELATED APPEALS AND INTERFERENCES

None.

Date of Deposit: September 23, 2003
I hereby certify under 37 CFR 1.8(a) that this correspondence is being deposited with the United States Postal Service as **first class mail** with sufficient postage on the date indicated above and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Cynthia L. Hayden

Cynthia L. Hayden

III. STATUS OF THE CLAIMS

Claims 1-18 are rejected. Each rejection is appealed.

IV. STATUS OF AMENDMENTS

All amendments have been entered.

V. SUMMARY OF THE INVENTION

In Figure 1, according to one embodiment, an adaptive filter 100 receives a video data stream 20 for performing filtering operations. The adaptive filter 100 may receive the video data stream 20 from a video decoder (not shown) or from an expansion port used to capture the video (not shown). See specification at page 3, line 19 through page 4, line 4.

In one embodiment, the video data stream 20 is a digital video stream. A digital video stream consists of video pixels being transmitted sequentially in the horizontal direction. Pixels are sent from left to right, then after one row is transmitted, the next row is sent until the entire image has been sent.

In one embodiment, the adaptive filter 100 receives the video data stream 20 into a first-in-first-out (FIFO) memory 18, before being received into a horizontal scaler 26. The horizontal scaler 26 produces a horizontally scaled video data stream 30.

In one embodiment, the horizontally scaled video data stream 30 is stored in a memory 22 of the adaptive filter 100. The memory 22 may be organized to facilitate access thereto, in some embodiments. For example, as shown in Figure 2, the memory 22 is divided into a plurality of line memories 48, wherein each line memory 48 is a predetermined length. In one

embodiment, the line memory 48 is an amount of memory that may store a single row of video data. See specification at page 4, line 5 through page 5, line 3.

Accordingly, the size of the line memory 48 may change upon receiving each new video data stream into the system 100. For example, for a video signal with a frame size of 720 x 480 comprising three bytes of data per pixel, the line memory 48 is 2160 bytes long (720 x 3). A video signal with 800 x 600 resolution frames which includes two bytes of data per pixel stores each row of data in a 1600-byte line memory 48 (800 x 2). The line memory 48 is dynamically adjusted to accept a row worth of video data, according to one embodiment.

A memory controller 24 is coupled to the memory 22, for controlling memory access. In one embodiment, the memory controller 24 may be programmed to change how rows of pixel data are both stored and retrieved in the line memories 48. In one embodiment, the memory controller 24 is programmed, based upon the scaling operation performed in the horizontal scaler 26, to facilitate efficient vertical scaling operations. Accordingly, a plurality of registers 32 are coupled to the memory controller 24. One register 32, for example, may identify the number of rows of pixel data stored in each line memory 48. A second register 32 may indicate offset addresses in the line memory 48 for accessing each row. These examples illustrate two of a number of uses for the registers 32 by the memory controller 24, to facilitate memory access before and after scaling operations.

In one embodiment, the memory 22 is coupled to a vertical scaler 36. In one embodiment, the scaled video data stream 40 is scaled in both the horizontal and vertical directions. See specification at page 5, lines 4 through 28.

A scaling control unit 28 is coupled to both the horizontal scaler 26 and the vertical scaler 36, for dynamically controlling the scaling operations in real time. In one embodiment, the

scaling control unit 28 is a processor-based system which controls the filter size (number of taps) for each of the horizontal and vertical scalers 26 and 36. The scaling control unit 28 further includes storage 16, such as for software 200 running in the scaling control unit 28.

In addition to controlling the horizontal scaler 26 and the vertical scaler 36, the scaling control unit 28 is coupled to the memory controller 24, for automatically changing the number of rows of pixel data that are stored in the memory 22.

In one embodiment, the adaptive filter 100 performs video scaling operations on the incoming video data stream 20. The adaptive filter 100 may thus be used where a video image is "down-sized," such as for supporting picture-in-picture (PIP), or to add additional graphics or other video data to the video image, such as display of stock quotes simultaneous with a television broadcast, for example.

According to one embodiment, the adaptive filter 100 may optimize the use of the memory 22 following a horizontal scaling operation by varying the density of stored information. By effectively increasing the available memory 22 accessible to the vertical scaler 36, the number of data samples 52 that may be stored in the memory 22 is increased. Accordingly, the size of the filter 70 in the vertical scaler 36 may be increased for performing vertical scaling. By increasing the size (e.g., the number of taps) of the vertical scaler 36 without increasing the amount of memory 22 needed to perform vertical scaling, the effective cost of the adaptive filter 100 is decreased while the quality of the filtered output signal 60 may actually improve.

In some prior art systems, an entire frame of video data may be stored in a frame buffer memory prior to performing any scaling or following the horizontal scaling operation. This results in at least one video frame of delay, which is not a real-time operation. Further, memory for storing an entire frame of video data is typically not small. For example, a video frame with

a resolution of 720 x 480 which stores three bytes per pixel is over one megabyte in size. On-board memories, however, typically store up to 2 kilobytes, 4 kilobytes, or 8 kilobytes of data.

In contrast, according to one embodiment, the adaptive filter 100 performs real-time operations during horizontal and vertical scaling. The operation to increase the density of stored data in the memory 22, following the horizontal scaling operation, is performed in real-time. Likewise, any adjustment to the size of the filter 70 in the vertical scaler 36 is made in real-time. Additionally, the adaptive filter 100 makes efficient use of the memory 22, making it possible for smaller memories, such as on-board memory, to be employed for performing these real-time operations. See specification at page 7, line 24 through page 8, line 19.

In Figures 4A-4C, pixels from the incoming video data stream 20 are stored in the memory 22 according to a typical prior art embodiment. Where no horizontal scaling is performed, e.g., 1:1 horizontal scaling, a first row 58 of the video data stream is stored in the first line memory 48, followed by a second row 58 stored in the second line memory 48, and so on, one row after another. For example, under the digital video standard described above, 720 pixels, corresponding to the first row 58 of the incoming video data stream 20, are stored in the first line memory 48 of the memory 22. Thus, there is direct correspondence between the line memory 58 number (e.g., first, second, third...) and the row 48 of the frame being stored.

Where the horizontal scaler 26 performs 2:1 horizontal scaling, the resulting pixels stored in the memory 22 occupy only half of the available space, as illustrated in Figure 4B. The first row 58 of video data is stored in the first line memory 48, as before. Because the row 58 occupies only half of the available line memory 48, a second row 58 may be stored in the first line memory 48. This is not what happens, however. Instead, the second row 58 is stored in the second line memory 48, not the first. As with 1:1 horizontal scaling, the first row 58 is stored in

the first line memory 48, the second row 58 is stored in the second line memory 48, the third row 58 is stored in the third line memory 48, and so on. Where 2:1 horizontal scaling is performed, half the available memory 22 is unused. Where 4:1 horizontal scaling is performed, only one-fourth of the memory 22 stores the pixel data, leaving three-fourths of the memory 22 empty, as depicted in Figure 4C.

According to one embodiment, the adaptive filter 100 optimizes the use of the memory 22 by increasing the density of data stored following horizontal scaling operations. For example, in Figure 5A, following 2:1 horizontal scaling, the first and second rows 58 are stored in the first line memory 48; the third and fourth rows 58 are stored in the second line memory 48; the fifth and sixth rows 58 are stored in the third line memory 48, and so on. Accordingly, twice as many rows 58 of pixel data are stored in each line memory 48 as during the 2:1 horizontal scaling operation described in Figure 4B. See specification at page 8, line 20 through page 9, line 21.

In Figure 5B, following a 3:1 scaling operation, the first, second and third rows 58 are stored in the first line memory 48, the fourth, fifth and sixth rows 58 are stored in the second line memory, and so on. Three times as many rows 58 are stored, in one embodiment, as when no scaling operation takes place. Likewise, in Figure 5C, four times as many rows 58 are stored in each line memory 48 following a 4:1 scaling operation.

In one embodiment, the adaptive filter 100 performs vertical scaling following the horizontal scaling operation. By first storing the pixels of the horizontally scaled video data stream 30 in the manner shown in Figures 5A-5C, the number of available data samples 52 to be used by the filter 70 of the vertical scaler 36 is increased. For example, in Figures 4A-4C, the same number of rows 58 is stored in the memory 22, whether horizontal scaling was performed or not. In each case, four rows 58 of pixel data, and thus four data samples 52, are available for

vertical scaling. In Figure 5A, however, because eight lines 58 are stored in the memory 22, eight data samples 52 are available for vertical scaling. Likewise, in Figures 5B and 5C, twelve and sixteen data samples 52, respectively, are available for scaling in the vertical direction.

The memory controller 24 controls accesses to and from the memory 22. In one embodiment, the scaling control unit 28 directs the memory controller 24 to change where each row 58 is stored, according to a prior horizontal scaling operation. Put another way, the number of rows 58 stored for each line memory 48 may be adjusted by the scaling control unit 28. In one embodiment, the registers 32 are updated by the scaling control unit 28 following horizontal scaling. The memory controller 24 may access the registers 32 to determine how subsequent accesses to the memory 22 are made. See specification at page 9, line 22 through page 10, line 16.

VI. ISSUES

A. Is Claim 1 Obvious Over Yeh In View Of May?

VII. GROUPING OF THE CLAIMS

All of the claims may be grouped with claim 1.

VIII. ARGUMENT

A. Is Claim 1 Obvious Over Yeh In View Of May?

Claim 1 calls for scaling a first and second portion of image information to provide a scaled first portion and a scaled second portion wherein unscaled first portion would

substantially fill a first memory area. The scaled first portion and the scaled second portion are stored in the first memory area.

The office action interprets first memory area to correspond to a single row of memory. Thus, it is noted that May teaches storing two scan lines in a single row of memory. However, in May, the single line of memory has the capacity to hold two scan lines, uncompressed. As shown in Figure 2a, a scan line includes 1024 bytes but the single row of memory in May holds 2048 bytes. Thus, May solves the problem by simply providing a relatively large memory.

However, this is not the solution set forth in the claim. The claim calls for scaling the first and second portion wherein, unscaled, the first portion would substantially fill the first memory area. Here, unscaled, neither the first portion or the second portion would substantially fill the memory area since they each only take up half of the memory area.

Thus, essentially May teaches away from the claimed invention of compressing so as to put two scan lines in a memory area adapted for one scan line. Instead, May teaches providing a memory of double capacity to take two scan lines.

The office action concedes that Yeh does not specifically teach storing the scaled first portion of the scaled second portion in the first memory area, wherein the unscaled portion would fill the first memory area. As pointed out above, May has the same deficiency.

In the Advisory Action, the Examiner addresses the comments in the Response to the Final Rejection, which comments are substantially those set forth above. The Applicant would like to make two points with respect to the comments in the Advisory Action. First, in the first paragraph of the Advisory Action, there is some misuse of language which probably is not important to the arguments the Examiner makes, but tends to make the arguments more confusing. In the first paragraph, in the second to last line, the Examiner indicates that Figure 2B

of the reference May teaches 2048 bytes per scan line. This is wrong. There is a 1024 bytes per scan line. This is clearly shown in Figure 2A and explained in the specification of May at column 2, lines 6 and 7. The point is that May teaches, in his discussion of the prior art, that two scan lines of 1024 pixels each may be stored in one memory row (Figure 2B) having a capacity of 2048 pixels. Thus, in the last line of the first paragraph of the Advisory Action it is indicated that a total number of row bytes of 2048 are able to be put in one scan line. Of course, this makes no sense at all. The Advisory Action is confusing scan lines and rows of memory. Perhaps it will help to point out that Figure 2B shows a 2048 pixel row line and Figure 2A shows a 1024 pixel scan line.

The second point goes to the way the Examiner is interpreting the claims. It is respectfully submitted that the interpretation of the claims the Examiner uses is unreasonable. For example, claim 1 calls for scaling a first portion and a second portion of image information to provide a scaled first portion and a scaled second portion. The claim goes on to state that, unscaled, the first portion would substantially fill a memory area. As always used in the office actions prior to the Advisory Action, the memory area was interpreted to be a memory row. In May, a memory row has a capacity of 2048 pixels or two scan lines. Thus, to read the claim on May, the first portion must be 2048 pixels. If May were to scale 2048 pixels two-to-one as suggested by the Examiner, he would then only have a scaled density in the memory line of 1024 pixels. May never teaches putting any more than the scaled 2048 pixels in a memory line, which is the crux of the present invention.

While the Examiner may contend that it is obvious to do what is claimed, all the art that the Examiner has found to date teaches away. Namely, no one has ever thought of using the

unused capacity within the memory line. It is indisputable that the claimed invention is extremely advantageous and in the face of teaching away, plainly unobvious.

The Examiner's misinterpretation of the claims is most plainly set forth in the third paragraph of the Advisory Action. There the Examiner argues that the Applicant states that in May, neither the unscaled first portion or the second portion would substantially fill the memory area. Hopefully the Applicant never made such an argument, because May never gets to a second portion. May only teaches putting the first portion, which is 2048 pixels, into a memory line. The Examiner, in the third paragraph, plainly interprets the unscaled first portion to have 1024 pixels but this is necessarily an incorrect reading of the claim.

As pointed out above, the claim defines what the first portion is. It is that amount of data which, unscaled, would "substantially fill a first memory area." The first memory area is agreed to be the memory line. But to fill the memory line in May you need 2048 pixels. Thus, the first portion is the entire 2048 pixels, since that is what fills the line unscaled.

The idea set forth in claim 1 is that you scale the 2048 down and then you add a second portion to fill up the remainder of the memory area now made available by scaling. This is what May plainly teaches away from.

The Examiner's attempt to simply read one scan line as the first portion and the other scan line as the second portion simply does not meet the terms of the claims and, therefore, amounts to an unreasonable claim construction.

Since the rejection is based on an unreasonable claim construction and a combination which teaches away from the claimed invention, claim 1 should be allowed.

Therefore, the rejection of claim 1 should be reversed.

IX. CONCLUSION

Applicant respectfully requests that each of the final rejections be reversed and that the claims subject to this Appeal be allowed to issue.

Respectfully submitted,

Date: September 23, 2003

Timothy N. Trop, Reg. No. 28,994
TROP, PRUNER & HU, P.C.
8554 Katy Freeway, Ste. 100
Houston, TX 77024
713/468-8880 [Phone]
713/468-8883 [Fax]

APPENDIX OF CLAIMS

The claims on appeal are:

1. A method comprising:

scaling a first portion and a second portion of image information to provide a scaled first portion and a scaled second portion, wherein unscaled said first portion would substantially fill a first memory area; and

storing said scaled first portion and said scaled second portion in said first memory area.

2. The method of claim 1, further comprising:

accessing the scaled first or second portion from the first memory area;

retrieving a data sample from the scaled portion; and

using the data sample in a second scaling operation.

3. The method of claim 1, further comprising:

dividing a memory into a plurality of lines;

identifying a line; and

storing a number of scaled portions in the line, wherein scaling the first portion and the second portion is based on a scaling ratio, and the number is related to the scaling ratio.

4. A system comprising:

a memory comprising a number of bytes;

a scaler to perform a scaling operation, the scaling operation identifiable by a scaling ratio, wherein the scaler scales a first portion and a second portion of image information to provide a scaled first portion and a scaled second portion, and unscaled said first portion would substantially fill a first memory area; and

a memory controller coupled to the memory to store said scaled first portion and said scaled second portion in said first memory area.

5. The system of claim 4, wherein the image information is a video data stream.

6. The system of claim 5, wherein the image information comprises a plurality of frames and each frame comprises a predetermined number of bytes.

7. The system of claim 6, wherein the number of bytes in the memory is smaller than the predetermined number of bytes.

8. The system of claim 4, wherein the scaling operation is a horizontal scaling operation.

9. The system of claim 4, further comprising:

a second scaler to perform a second scaling operation, identifiable by a second scaling ratio.

10. The system of claim 9, wherein the second scaling ratio is identical to the first scaling ratio.

11. The system of claim 9, wherein the second scaling operation is a vertical scaling operation.

12. The system of claim 9, further comprising:

a scaling control unit coupled to the second scaler, wherein the second scaler further comprises a finite impulse response filter including a plurality of coefficients and the scaling control unit changes the amount of coefficients in the filter in relation to the scaling ratio.

13. The system of claim 12, wherein the scaling control unit further comprises a look-up table including coefficient values for changing the amount of coefficients.

14. The system of claim 4, further comprising a first-in-first-out memory.

15. The system of claim 4, wherein the memory is an on-chip memory.

16. An article comprising a medium storing instructions that, if executed, enable a processor-based system to:

scale a first portion and a second portion of image information to provide a scaled first portion and a scaled second portion, wherein unscaled said first portion would substantially fill a first memory area; and

store said scaled first portion and said scaled second portion in said first memory area.

17. The article of claim 16, further storing instructions that, if executed, enable a processor-based system to:

access the scaled first or second portion from the first memory area;

retrieve a data sample from the scaled portion; and

use the data sample in a second scaling operation.

18. The article of claim 16, further storing instructions that, if executed, enable a processor-based system to:

divide a memory into a plurality of lines;

identify a line of the plurality of lines; and

store a number of scaled portions in the line, wherein scaling the first portion and the second portion is based on a scaling ratio, and the number is related to the scaling ratio.

TRANSMITTAL OF APPEAL BRIEF (Large Entity)	Docket No. ITL.0447US

In Re Application Of: **Paul S. Gryskiewicz**

Serial No.	Filing Date	Examiner	Group Art Unit
09/652,694	August 31, 2000	Brian P. Yenke	2614

Invention: **Adaptive Video Scaler**

TO THE COMMISSIONER FOR PATENTS:

Transmitted herewith in triplicate is the Appeal Brief in this application, with respect to the Notice of Appeal filed on **September 3, 2003.**

The fee for filing this Appeal Brief is: **$320.00**

☒ A check in the amount of the fee is enclosed.

☐ The Director has already been authorized to charge fees in this application to a Deposit Account.

☒ The Director is hereby authorized to charge any fees which may be required, or credit any overpayment to Deposit Account No. **20-1504**

Signature

Dated: **September 23, 2003**

Timothy N. Trop, Reg. No. 28,994
Trop, Pruner & Hu, P.C.
8554 Katy Freeway, Suite 100
Houston, Texas 77024
(713) 468-8880
(713) 468-8883 (fax)

I certify that this document and fee is being deposited on **09-23-03** with the U.S. Postal Service as first class mail under 37 C.F.R. 1.8 and is addressed to the Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Cynthia L. Hayden

Signature of Person Mailing Correspondence

Cynthia L. Hayden

Typed or Printed Name of Person Mailing Correspondence

cc: